-- Figs. 2a to 2e are partial, diagrammatic sectional views of structures illustrating further process steps for fabricating a microelectronic structure; --

Please replace the paragraph on page 25, lines 2-14 with the following paragraph.

-- Process steps for fabricating a microelectronic structure with a metal silicide layer on the base substrate in accordance with a further exemplary embodiment are illustrated in Figs. 2a to 2e. In this case, too, the process proceeds from a base substrate 5, which may optionally also be constructed from two layers. To that end, the base substrate 5 includes a lower silicon dioxide layer 50 with a silicon nitride or TEOS layer 55 situated above it. The base substrate 5 furthermore has a contact hole 10, which is filled with polysilicon up to the surface 15 of the base substrate 5. First of all, after cleaning with hydrofluoric acid, a platinum, titanium or cobalt silicide layer having a thickness of between 30 and 100 nm is applied to this structure illustrated in Fig. 2a. --